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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,024	07/31/2003	Gerard Chauvel	TI-35461 (1962-05418)	9347

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EXAMINER	
WEINTROP, ADAM S	
ART UNIT	PAPER NUMBER
2109	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/632,024	CHAUVEL ET AL.	
	Examiner	Art Unit	
	Adam S. Weintrop	2109	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/31/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

The application or patent numbers are missing from page 1 and 2 of the specification. Applicant needs to fill in these blanks with the correct numbers in order to successfully incorporate by reference the named references.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 1-3, 7, 9-10, 12, 21, and 24** are rejected under 35 U.S.C. 102(e) as being anticipated by Evoy et al. (US 6,766,460).

Regarding **claim 1**, Evoy et al. anticipates a system, comprising: a first processor that executes a transaction targeting a pre-determined address (column 6, lines 15-30, where a host processor initiates a Java application, thus informing the power management system, seen as a predetermined address); a second processor coupled

to said first processor (Figure 1, with the master processor and the slave processor both coupled to the system bus); and a wait unit coupled to said first and second processors, said wait unit detects said pre-determined address and asserts a wait signal to cause said first processor to enter a wait mode (column 6, lines 15-35, where the power management system detects the transaction to the Java processor, seen as a predetermined address, and subsequently signals the host process to power down, seen as a wait state).

Regarding **claim 2**, Evoy et al. anticipates the system of claim 1, wherein the wait signal is de-asserted to permit the first processor to retrieve a status of the second processor (column 6, line 62 - column 7, line 10, where the Java completion signal is sent to bring the host processor out of its wait state and therefore the host processor retrieves completion status of the Java processor simply by receiving the Java completion signal).

Regarding **claim 3**, Evoy et al. anticipates the system of claim 2, wherein the status includes one or more instructions that the first processor is to execute (column 10, line 65 - column 11, line 17, with in Operation 214, post process operations are executed based on the Java completion signal status message returning to the first processor).

Regarding **claim 7**, Evoy et al. anticipates the system of claim 1, wherein said wait unit de-asserts the wait signal upon detection of a signal from said second process (column 7, lines 4-7, where after receiving the completion signal from the Java processor, the host processor's wait status is de-asserted).

Regarding **claim 9**, Evoy et al. anticipates a method, comprising: executing a transaction that targets a pre-determined address (column 6, lines 15-30, where a host processor initiates a Java application, thus informing the power management system, seen as a predetermined address); detecting the transaction to said pre-determined address; asserting a wait signal upon detection of the transaction to cause a processor to stall (column 6, lines 15-35, where the power management system detects the transaction to the Java processor, seen as a predetermined address, and subsequently signals the host process to power down, seen as a wait state); causing said wait signal to de-assert upon occurrence of an event (column 6, line 62 - column 7, line 10, where the Java completion signal is sent to bring the host processor out of its wait state), said de-assert controlled by logic external to said processor (column 7, lines 4-10, where the host processor goes back to normal, seen as de-asserting the wait signal, and this is caused by the Java completion signals and the host register switch 56, external to the processor itself as seen in Figure 2).

Regarding **claim 10**, Evoy et al. anticipates the method of claim 9 wherein said stall comprises a low power mode (column 6, lines 23-27, where the host processor goes to a lower power when processing is transferred over to the slave processor with the Java mode signal)

Regarding **claim 12**, Evoy et al. anticipates the method of claim 9 wherein said event comprises a signal from another processor (column 6, line 62 - column 7, line 7, where after the slave processor halts execution, the receiving of the completion signal

from the Java processor's registers occurs and the host processor's wait status is de-asserted).

Regarding **claim 21**, Evoy et al. anticipates a system, comprising; a first processor; a second processor; means for detecting a transaction targeting a pre-determined address (column 6, lines 15-30, where a host processor initiates a Java application, thus informing the power management system, seen as a predetermined address, Figure 1, with the master processor and the slave processor both coupled to the system bus) and for asserting a wait signal to said first processor to cause the first processor to enter a wait state (column 6, lines 15-35, where the power management system detects the transaction to the Java processor, seen as a predetermined address, and subsequently signals the host process to power down, seen as a wait state); and means for releasing said first processor from the wait state (column 6, line 62 - column 7, line 10, where the Java completion signal is sent to bring the host processor out of its wait state).

Regarding **claim 24**, Evoy et al. anticipates the system of claim 21 wherein said means for releasing said first processor from the wait state comprises a wait release signal from said second processor coupled to a wait unit, said wait unit de-asserts the wait signal upon detection of the wait release signal (column 7, lines 4-10, where the host processor goes back to normal, seen as de-asserting the wait signal, and this is caused by the Java completion signals from the slave processor and the host register switch 56, external to the processors, seen as part of a wait unit as seen in Figure 2).

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 15 and 18** are rejected under 35 U.S.C. 102(b) as being anticipates by Miller et al. (US 5,596,759).

Regarding **claim 15**, Miller et al. anticipates a wait unit, comprising: a decode logic unit that determines when a first processor runs a transaction to a pre-determined address (column 5, line 57 - column 6, line 5, where the interprocessor logic includes sleep bits which set sleep status for each processor, therefore a request to start the second processor from the first processor, seen as a transaction to a predetermined address, is permitted only by the interprocessor logic since it defines the sleep bits of each processor, thereby determining the instances where processors can interact with each other); a first processor interface; a second processor interface (Figure 1, where the interprocessor logic is coupled to both processors); logic coupled to the decode logic unit, the first processor interface, and the second processor interface, wherein said logic asserts a signal propagated by the first processor interface to cause said processor to stall (column 10, lines 12-45, where interactions with the interprocessor logic allow the first processor to activate the second processor and once the second processor is activated then the first processor waits for completion signals from the second processor as seen in Figure 4).

Regarding **claim 18**, Miller et al. anticipates the wait unit of claim 15 wherein said second processor interface receives a wait release signal from a second processor that causes the wait unit to de-assert the wait signal to said first processor through said first processor interface (column 9, lines 4-53, where the status bits in the processor option register, seen as part of a wait unit are accessed and manipulated during processor activations and when the second processor is completed processing, the bits are changed to allow the first process to acknowledge the completion and resume out of its own wait state).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 4-5, 13-14, and 22-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Evoy et al. (US 6,766,460) in view of Shenk (US 4,535,404).

Regarding **claims 4-5, 13-14, and 22-23**, Evoy et al. discloses all of the limitations as described above except for having the transactions comprise a memory read or a memory write to or from the predetermined address. The general concept of reading or writing to memory in order to activate certain peripherals is well known in the art as illustrated by Shenk. Shenk discloses a system of memory mapped I/O. Memory mapped I/O allows for peripheral devices to be controlled by referencing memory with

normal program instructions and the memory is set aside by a predetermined amount of space and addressing within this space (column 1, lines 13-50, with reading or writing interpreted as a normal memory reference instruction). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Evoy et al. with using memory mapped I/O in order to increase the flexibility of I/O programming as noted in Shenk's disclosure in column 1, lines 50-52).

8. **Claims 6, 11, and 25** are rejected under 35 U.S.C. 103(a) as being unpatentable over Evoy et al. (US 6,766,460) in view of Mustafa et al. (US 6,678,830).

Regarding **claims 6, 11, and 25**, Evoy et al. discloses all of the limitations except for waking the first processor (de-asserting the wait signal) in response to a system interrupt. The general concept of activating processors from any sleep state in response to a system wide interrupt is well known in the art as illustrated by Mustafa et al. Mustafa et al. describes a keyboard controller that activates computers. This activation is used as an interrupt, and is interpreted as a "system interrupt" since it can activate the processor from an I/O device (column 2, lines 5-30). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Evoy et al. with using a system interrupt to activate a processor as taught by Mustafa et al. in order to take advantage of power management functionalities as noted in Mustafa's disclosure in column 1, lines 39-41.

9. **Claim 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Evoy et al. (US 6,766,460) in view of Johnson, Jr. et al. (US 4,420,806).

Regarding **claim 8**, Evoy et al. discloses all of the limitations as described above except for having the wait unit, upon detection of said signal, assert a processor interrupt signal to the first processor if the wait signal is already de-asserted. Johnson, Jr. et al. describes that inter-processor interrupts are employed when a processor requires the services of another processor. When the wait unit detects that the wait signal is already de-asserted, this can only happen from a system interrupt occurring, such as an interrupt generated by external I/O. If the first processor is already activated, and the second processor needs the services of the first processor, the second processor can implement an interprocessor interrupt as described in Johnson, Jr. et al. in order to request the first processor to execute the tasks which the second processor needs executed (column 1, lines 17-26). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Evoy et al. with using interprocessor interrupts to request the attention of a processor that is already involved in another task as taught by Johnson, Jr. et al. in order to facilitate the implementation of integrating multiple processors together as to increase speed and reduce the size of components as noted in Johnson, Jr. et al.'s disclosure in column 1, lines 11-17.

10. **Claims 16-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (US 5,596,759) in view of Shenk (US 4,535,404).

Regarding **claims 16-17**, Miller et al. discloses all of the limitations as described above except for having the transactions comprise a memory read or a memory write to or from the predetermined address. The general concept of reading or writing to memory in order to activate certain peripherals is well known in the art as illustrated by

Shenk. Shenk discloses a system of memory mapped I/O. Memory mapped I/O allows for peripheral devices to be controlled by referencing memory with normal program instructions and the memory is set aside by a predetermined amount of space and addressing within this space (column 1, lines 13-50, with reading or writing interpreted as a normal memory reference instruction). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Miller et al. with using memory mapped I/O in order to increase the flexibility of I/O programming as noted in Shenk's disclosure in column 1, lines 50-52).

11. **Claim 19** is rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (US 5,596,759) in view of Johnson, Jr. et al. (US 4,420,806).

Regarding **claim 19**, Miller et al. discloses all of the limitations as described above except for having the wait release signal cause a processor interrupt signal to be asserted if the wait signal is already de-asserted. Johnson, Jr. et al. describes that inter-processor interrupts are employed when a processor requires the services of another processor. When the wait unit detects that the wait signal is already de-asserted, this can only happen from a system interrupt occurring, such as an interrupt generated by external I/O. If the first processor is already activated, and the second processor needs the services of the first processor, the second processor can implement an interprocessor interrupt as described in Johnson, Jr. et al. in order to request the first processor to execute the tasks which the second processor needs executed (column 1, lines 17-26). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Miller et al. with using interprocessor interrupts

to request the attention of a processor that is already involved in another task as taught by Johnson, Jr. et al. in order to facilitate the implementation of integrating multiple processors together as to increase speed and reduce the size of components as noted in Johnson, Jr. et al.'s disclosure in column 1, lines 11-17.

12. **Claim 20** is rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (US 5,596,759) in view of Mustafa et al. (US 6,678,830).

Regarding **claim 20**, Miller et al. discloses all of the limitations except for waking the first processor (de-asserting the wait signal) in response to a system interrupt. The general concept of activating processors from any sleep state in response to a system wide interrupt is well known in the art as illustrated by Mustafa et al. Mustafa et al. describes a keyboard controller that activates computers. This activation is used as an interrupt, and is interpreted as a "system interrupt" since it can activate the processor from an I/O device (column 2, lines 5-30). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Miller et al. with using a system interrupt to activate a processor as taught by Mustafa et al. in order to take advantage of power management functionalities as noted in Mustafa's disclosure in column 1, lines 39-41.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adam S. Weintrop whose telephone number is 571-270-

1604. The examiner can normally be reached on Monday through Friday 7:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frantz Jules can be reached on 571-272-6681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AW 4/9/07

FRANTZ JULES
SUPERVISORY PATENT EXAMINER

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